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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER

SANDOVAL, PATRICK

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PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 10/596,944	Applicant(s) MAZIASZ ET AL.	
	Examiner PATRICK SANDOVAL	Art Unit 2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 28 July 2009 and 30 October 2009.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 36-47 and 71-78, wherein claims 48-70 are cancelled is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 36-47 and 71-78 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. This Office Action responds to Applicant's RCE filed 7/28/2009 and election filed 10/30/2009. Claims 36-47 have been elected, claims 48-70 have been cancelled, and claims 71-78 have been added. Claims 36-47 and 71-78 are pending.

Continued Examination Under 37 CFR 1.114

2. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 7/28/2009 has been entered.

Election/Restrictions

3. Applicant's election without traverse of Claims 36-47 in the reply filed on 10/30/2009 is acknowledged. Non-elected claims 48-70 have been cancelled.

4. Applicant is reminded that upon cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a request under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

Response to Amendment

5. Applicant's arguments with respect to claims 36-47 and 71-78 have been considered but are moot in view of the new ground(s) of rejection in view of previously

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cited but not relied upon prior art references Gupta (US 6,163,877) and McGuinness et al. (McGuinness) (US2004/0078768).

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. **Claims 36-47 and 71-78 are rejected** under 35 U.S.C. 102(b) as being anticipated by Gupta (US 6,163,877).

8. **Claims 36-47 and 71-78 are rejected** under 35 U.S.C. 102(e) as being anticipated by McGuinness et al. (McGuinness) (US2004/0078768).

9. The applied reference McGuinness has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention “by another,” or by an appropriate showing under 37 CFR 1.131.

10. McGuinness and/or Gupta disclose:

11. (Claims 36, 46 and 47) A method comprising:

selecting at the computer device a first portion of a first transistor of the circuit layout in response to determining the first portion extends outward in a first direction from a first logical device of the circuit layout, the first logical device comprising the first transistor, and in response to selecting the first portion, reshaping at the computer device the first transistor to reduce a size of the first logical device in the first direction (McGuinness, Paragraphs 47-48, transistor fitting within transistor boundaries such as a height template constraint) (Gupta, Col. 7, ll. 33-40, Fig. 9, wherein large transistors exceeding a certain height are folded);

reshaping at the computer device a second portion of the first logical device in response to reducing the size of the first logical device (McGuinness, Paragraphs 47-48, wherein reduction of one finger size height of a folded transistor is compensated by increases in other finger sizes, Paragraph 57, Figs. 10-13) (Gupta, Col. 4, ll. 44-67 – Col. 5, ll. 1-7, Fig. 5, wherein transistor folding a transistor finger is reduced or removed and replaced with two fingers to meet cell height requirements);

similarly reducing the size of a second logical device in the first direction by reshaping third and fourth portions of the second logical device (McGuinness, Paragraphs 47-48, transistor fitting, finger size reduction compensated by increase in other finger sizes) (Gupta, Fig. 9 and applicable text, wherein all large transistors exceeding height limits are folded); and

reshaping/resizing transistor portions in a second direction (McGuinness, Paragraphs 28, 30 and 35) (Gupta, Claim 3, wherein transistor width requirements are also taken into consideration).

12. (Claim 37 and 71) Wherein the first portion of the first transistor comprises a first transistor finger, and the third portion of the second transistor comprises a first transistor finger (McGuinness, Paragraphs 47-48, Paragraph 57, Figs. 10-13) (Gupta, Fig. 5 and applicable text).

13. (Claim 38 and 72) Wherein the second portion of the first logical device comprises a second transistor finger of the first transistor and wherein the fourth portion of the second transistor comprises a second transistor finger of the second transistor (McGuinness, Paragraphs 47-48, Paragraph 57, Figs. 10-13) (Gupta, Col. 4, ll. 44-67 – Col. 5, ll. 1-7, Fig. 5, wherein transistor folding a transistor finger is reduced or removed and replaced with two fingers to meet cell height requirements).

14. (Claim 39 and 73) Wherein the second portion of the first logical device comprises a transistor finger of a second transistor and wherein the fourth portion comprises a transistor finger of a third transistor (McGuinness, Paragraphs 47-48, Paragraph 57, Figs. 10-13) (Gupta, Col. 4, ll. 44-67 – Col. 5, ll. 1-7, Fig. 5, wherein transistor folding a transistor finger is reduced or removed and replaced with two fingers to meet cell height requirements).

15. (Claims 40, 74 and 78) Wherein reshaping the first/third portion comprises reducing a size of the first transistor finger (McGuinness, Paragraphs 47-48, finger size reduction, Paragraph 57, Figs. 10-13) (Gupta, Col. 4, ll. 44-67 – Col. 5, ll. 1-7, Fig. 5,

wherein transistor folding a transistor finger is reduced or removed and replaced with two fingers to meet cell height requirements).

16. (Claims 41 and 75) Wherein reshaping the first/third portion comprises removing the first transistor finger (McGuinness, Paragraphs 47-48, wherein reduction of one finger size height of a folded transistor is compensated by increases in other finger sizes, Paragraph 57, Figs. 10-13) (Gupta, Col. 4, ll. 44-67 – Col. 5, ll. 1-7, Fig. 5, wherein transistor folding a transistor finger is reduced or removed and replaced with two fingers to meet cell height requirements).

17. (Claims 42 and 76) Wherein reshaping the first/third portion comprises rotating the first transistor (wherein layout/cell compaction it is well known to rotate/move/alter ratios/shapes as needed to improve the overall layout area).

18. (Claims 43 and 77) Reshaping a third portion of the first logical device in response to reducing the size of the first transistor portion (McGuinness, Paragraphs 47-48, wherein reduction of one finger size height of a folded transistor is compensated by increases in other finger sizes, Paragraph 57, Figs. 10-13) (Gupta, Col. 4, ll. 44-67 – Col. 5, ll. 1-7, Fig. 5, wherein transistor folding a transistor finger is reduced or removed and replaced with two fingers to meet cell height requirements).

19. (Claims 44 and 45) Storing a first state associated with the circuit layout at the computer device in response to selecting the first portion of the first transistor; in response to reshaping the first portion of the first transistor, determining if a size of the circuit layout has been reduced in the first direction (McGuinness, Paragraphs 26 and 29, Fig. 2, wherein each fold solution is selected and used in turn to generate a possible

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layout to generate a final optimized cell layout solution, wherein layout height is compared to cell height constraint) (Gupta, Fig. 9 #914 and related text, wherein a best solution is selected); and

in response to determining the size of the circuit layout has not been reduced, restoring the circuit layout to the first state (McGuinness, Paragraph 29, wherein the best optimized layout is chosen) (Gupta, Fig. 9 #914 and related text, wherein a best solution is selected) (wherein it is inherent in layout optimization that if a proposed solution does not meet cell height constraints it would not be a valid solution).

Remarks

20. The rejections of claims 1-7, 9-15 and 18-35 under 35 U.S.C. 112, second paragraph and the objections to claims 1-7, 9-15 and 18-35 have been removed in light of Applicant's amendment filed 7/28/2009 cancelling claims 1-35.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to PATRICK SANDOVAL whose telephone number is (571)272-7973. The examiner can normally be reached on 8:00 am to 5:30 pm Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571-272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Paul Dinh/
Primary Examiner, Art Unit 2825

/Patrick Sandoval/
Examiner, Art Unit 2825